TEXAS INSTRUMENTS

THS7530EVM

User's Guide

April 2003 *High Performance Linear Products*

SLOU161

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the specified input and output ranges described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Chapter 1

Description

This chapter gives a general description of the THS7530EVM.

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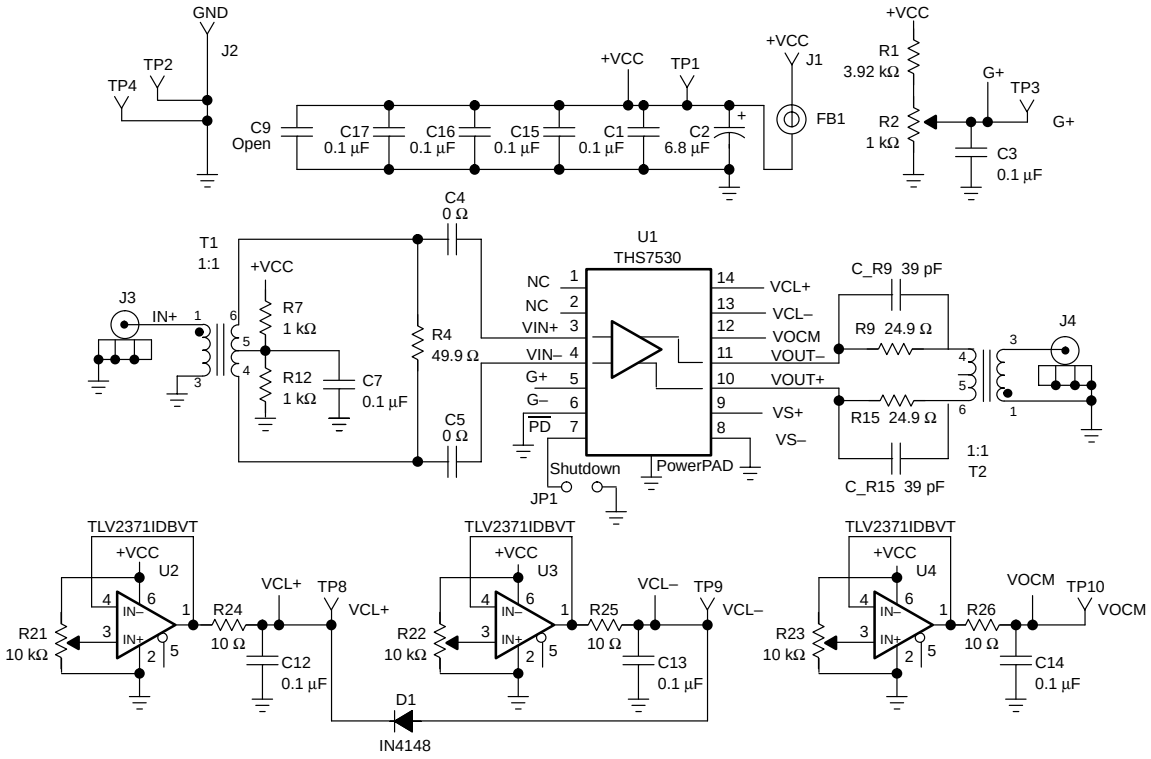
1.1 General Description

The THS7530 is a dc-coupled wide bandwidth amplifier with voltage-controlled gain. The amplifier has high impedance differential inputs and low impedance differential outputs with high bandwidth gain control, output common mode control, and output voltage clamping. It is packaged in a 14-pin PWP PowerPAD™ package. The schematic of the THS7530EVM, as furnished, is shown in Figure 1–1.

Figure 1–1. THS7530EVM Schematic



1.2 Board Description

- ❏ Power input: +5Vdc at +Vcc (J1), test point TP1
- ❏ Common reference: GND (J2), test point TP2 and TP4
- ❏ Signal input: IN+ (J3)
- ❏ Signal output: OUT– (J4)
- ❏ Gain control: Gain (R2), test point TP3
- ❏ High clamp voltage: VCL+ (R21), test point TP8
- ❏ Low clamp voltage: VCL– (R22), test point TP9
- ❏ Output common–mode voltage: VOCM (R23), test point TP10
- ❏ Power down: $\overline{\text{SHD}}$ (JP1) open for normal operation (Pin labeled $\overline{\text{PD}}$ in the data sheet).

PowerPAD is a trademark of Texas Instruments.

Chapter 2

THS7530EVM Design

This chapter discusses general design considerations for theTHS7530EVM.

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2.1 General Design Considerations

The THS7530 is designed for nominal 5-V power supply from V_{S+} to $V_{S–}$.

The amplifier has fully differential inputs, V_{IN+} and $V_{IN–}$, and fully differential outputs, V_{OUT+} and $V_{OUT–}$. The inputs are high impedance and outputs are low impedance. External resistors are required for impedance matching and termination purposes.

For best performance, the input and output common-mode voltage should be maintained at the midpoint between V_{S+} and $V_{S–}$. The output common-mode voltage is controlled by the voltage applied to V_{OCM}. If left unconnected, V_{OCM} is set at mid-rail by internal resistors. The input common-mode voltage must be set by external means.

Voltage applied from $V_{G–}$ to V_{G+} controls the gain of the part with 38.8 dB/V gain compliance. The input can be differential or single-ended. $V_{G–}$ must be maintained within ±0.8 V of $V_{S–}$.

V_{CL+} and $V_{CL–}$ are inputs that limit the output voltage swing of the amplifier. The voltages applied set an absolute limit on the voltages at the output.

$\overline{PD}$ input controls the power down feature of the part. A TTL low puts the part into power savings mode, and a high or unconnected input puts the part in normal operating mode.

Power supply bypass capacitors are required for proper operation. A 6.8-µF tantalum bulk capacitor is recommended if the amplifier is located far from the power supply and may be shared among other devices. A ceramic 0.1-µF capacitor is recommended within 0.1″ of the device power pin. The ceramic capacitor should be located on the same layer as the amplifier to eliminate the use of vias between the capacitors and the power pin if possible.

2.2 Other Circuits

Figures 2–1 through 2–4 show some different variations of circuit configurations that can be built by modifying the EVM.

Figure 2–1. AC-Coupled Single-Ended Input With AC-Coupled Differential Output

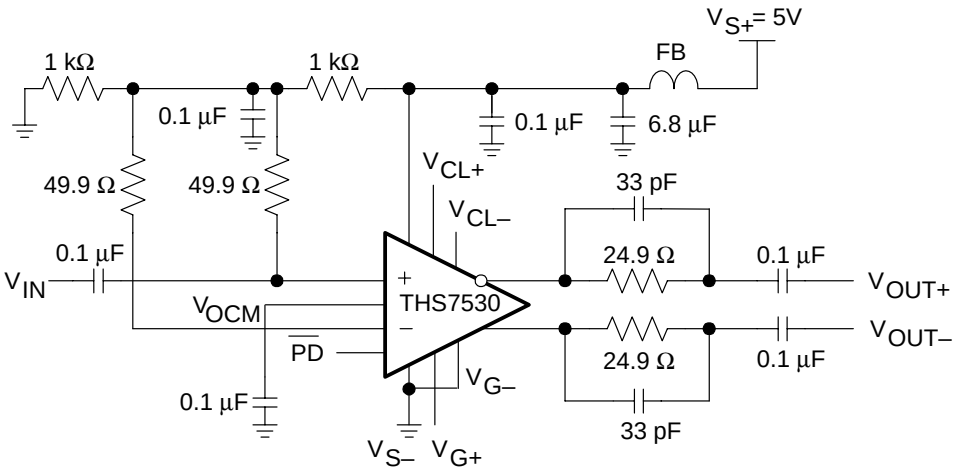


Figure 2–2. AC-Coupled Differential Input With AC-Coupled Differential Output

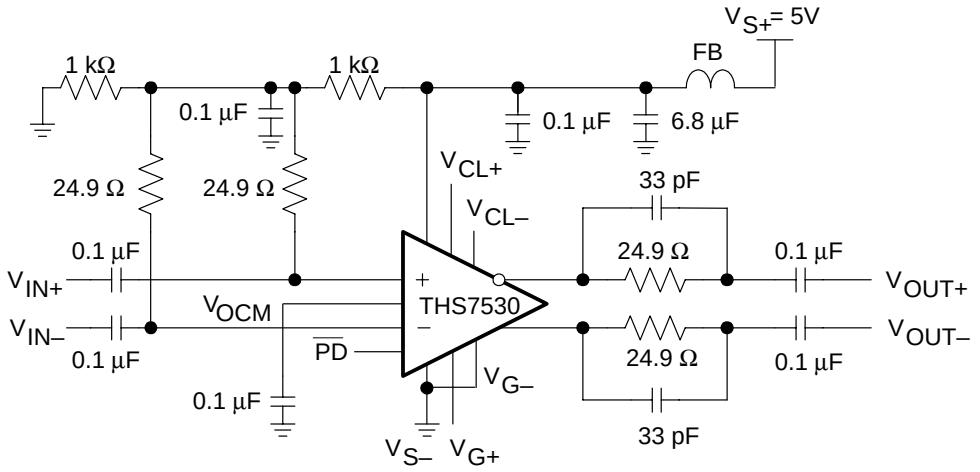


Figure 2–3. DC-Coupled Single-Ended Input With DC-Coupled Differential Output

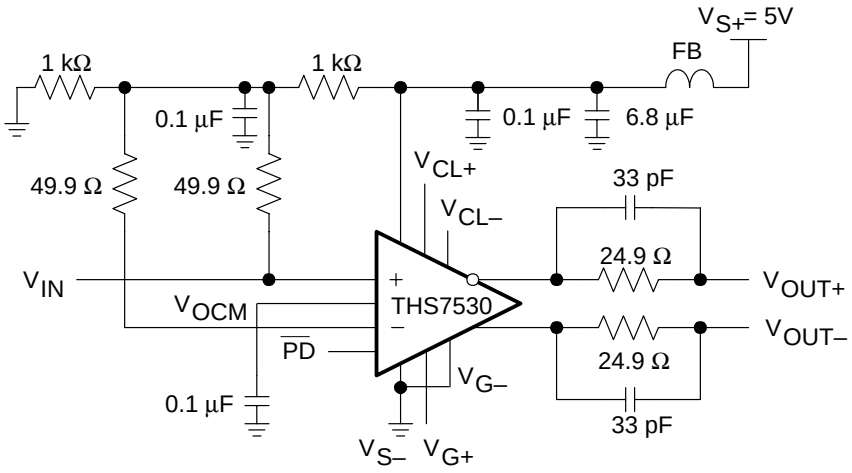
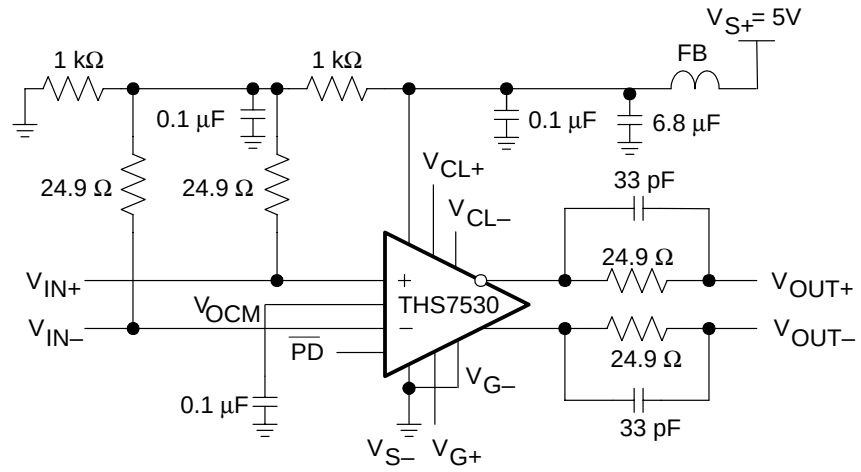


Figure 2–4. DC-Coupled Differential Input With DC-Coupled Differential Output



Chapter 3

EVM Schematic and Bill of Materials

This chapter provides a complete schematic diagram, board layouts, and bill of materials for the THS7530EVM.

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3.1 Complete EVM Schematic

Figure 3–1. Complete EVM Schematic

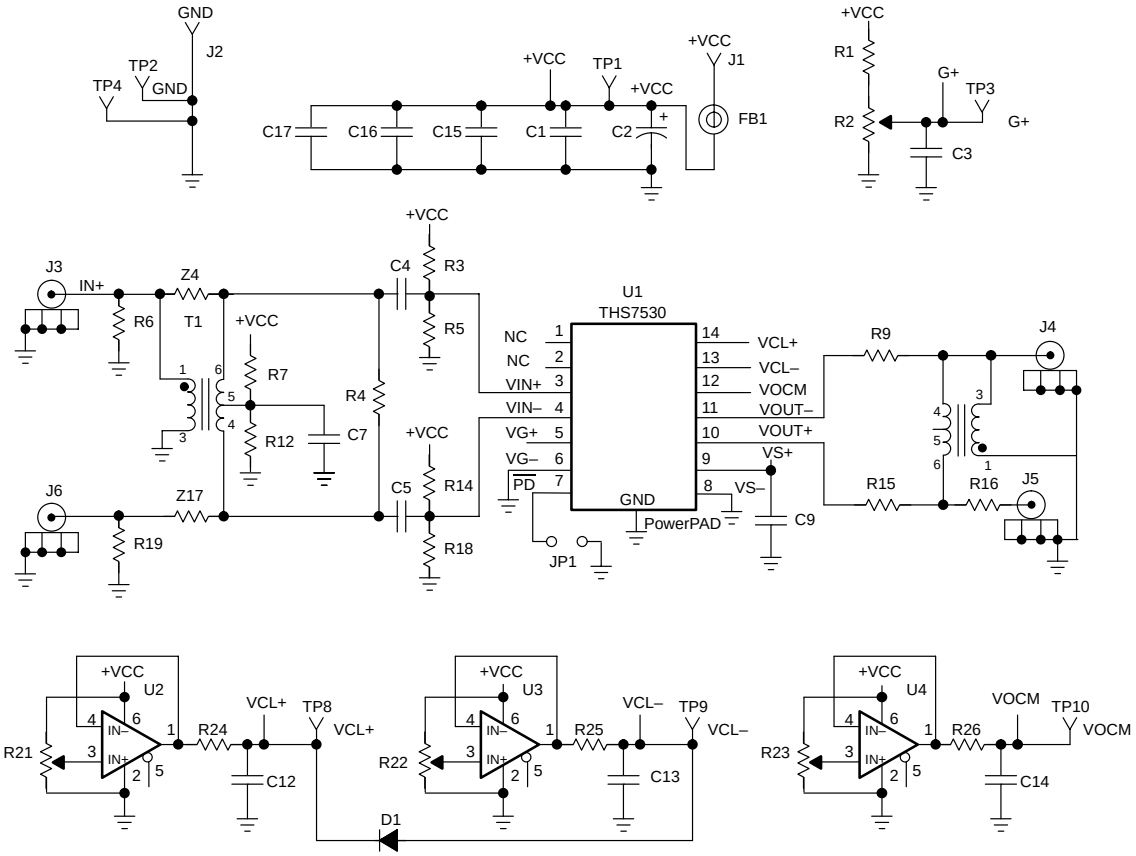
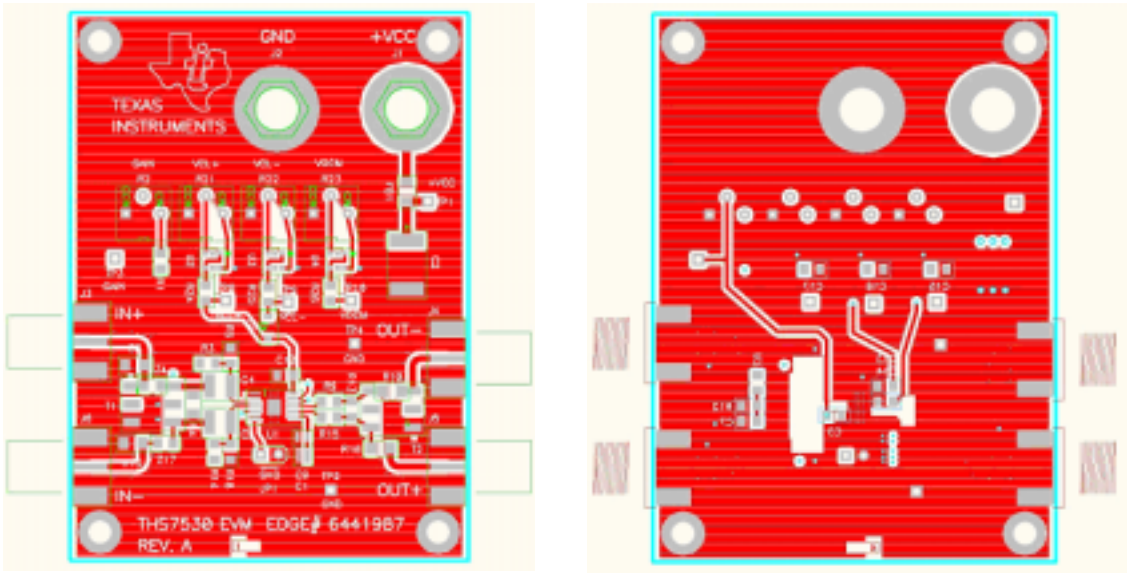


Figure 3–2. EVM Board Layout: Top (Left) and Bottom (Right)



3.2 EVM Bill of Materials

Item	Description	Size	Ref Des	Qty	Part Number
1	Bead, ferrite, 3 A, 80 Ω	1206	FB1	1	(Steward) HI1206N800R–00
2	Capacitor, tantalum, 6.8 µF, 35 V, 10%	D	C2	1	(AVX) TAJD685K035R
3	Capacitor, ceramic, 0.1 µF, X7R, 16V	0508	C1	1	(AVX) 0508YC104KAT2A
5	Capacitor, ceramic, 0.1 µF, X7R, 50 V	0805	C3, C7, C12, C13, C14, C15, C16, C17	8	(AVX) 08055C104KAT2A
6	Diode, Schottky, 20 V, 0.5 A	SOD-123	D1	1	(Diodes Inc.) B0520LW–7
7	Resistor, 10 Ω, 1/8 W, 1%	0805	R24, R25, R26	3	(PHYCOMP) 9C08052A10R0FKHFT
8	Resistor, 24.9 Ω, 1/8 W, 1%	0805	R9, R15	2	(PHYCOMP) 9C08052A24R9FKHFT
9	Resistor, 1 kΩ, 1.8W, 1%	0805	R7, R12	2	(PHYCOMP) 9C08052A1001FKHFT
10	Resistor, 3.92 kΩ , 1/8 W, 1%	0805	R1	1	(PHYCOMP) 9C08052A3921FKHFT
11	Resistor, 0 Ω, 1/4 W	1206	C4, C5	2	(PHYCOMP) 9C12063A0R00JLHFT
12	Resistor, 49.9 Ω, 1/4 W, 1%	1206	R4	1	(PHYCOMP) 9C12063A49R9FKRFT
13	Pot., ceramic, 1/4 inch square, 1 kΩ		R2	1	(Bourns) 3362P–1–102
14	Pot., ceramic, 1/4 inch square, 10 kΩ		R21, R22, R23	3	(Bourns) 3362P–1–103
15	IC, TLV2371	SOT-23	U2, U3, U4	3	(TI) TLV2371IDBVT
16	Transformer, 1:1	CD542	T1, T2	2	(Mini-Circuits) ADT1-1WT
17	Connector, edge, SMA PCB Jack		J3, J4	2	(Johnson) 142–0701–801
18	Jack, banana receptacle, 0.25” diameter hole		J1, J2	2	(HH Smith) 101
19	Header, 0.1” Ctrs, 0.025” square pins	2 POS.	JP1	1	(Sullins) PZC36SAAN
20	Shunts		JP1	1	(Sullins) SSC02SYAN
21	Test point, black		TP2, TP3, TP4	3	(Keystone) 5001
22	Test points, red		TP1, TP8, TP9, TP10	4	(Keystone) 5000
23	Standoff, 4–40 Hex, 0.625” Length			4	(Keystone) 1804
24	Screw, Phillips, 4–40, .250”			4	SHR–0440–016–SN
25	IC, THS7530		U1	1	(TI) THS7530PWP
26	Board, printed circuit			1	(TI) EDGE # 6441987